REMARKS

The present application was filed on August 28, 2003 with claims 1-17. Claims 1, 6, 11 and 12 are the independent claims.

In the outstanding Office Action, the Examiner: (I) rejected claims 1, 4-6, 9-12 and 17 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 4,627,057 to Schmidt et al. (hereinafter "Schmidt"); (ii) rejected claims 2 and 7 under 35 U.S.C. §103(a) as being unpatentable over Schmidt in view of U.S. Patent No. 5,282,211 to Manlick et al. (hereinafter "Manlick"); (iii) rejected claims 3 and 8 under 35 U.S.C. §103(a) as being unpatentable over Schmidt in view of U.S. Patent No. 6,215,876 to Gilley (hereinafter "Gilley");" (iv) rejected claims 13-17 under 35 U.S.C. §103(a) as being unpatentable over Schmidt in view of U.S. Patent Application Publication No. 2002/0063553 to Jungerman (hereinafter "Jungerman"); and (v) rejected claims 1, 6 and 11 under 35 U.S.C. §103(a) as being unpatentable over Jungerman in view of Schmidt.

In this response, Applicants: (I) amend claims 1, 2, 6, 7 and 11; and (ii) traverse the §102(b) and §103(a) rejections for at least the following reasons.

While Applicants believe that the original claims of the present application are patentable over Schmidt, Manlick, Gilley and Jungerman, alone or in combination, Applicants have nonetheless amended claims 1, 2, 6, 7 and 11 in a sincere effort to expedite the present application through to issuance. Support for the amendments may be found throughout the present application, by way of example only, see page 6, line 10, through page 8, line 7.

Regarding the §102(b) rejection based on Schmidt, Applicants respectfully assert that Schmidt fails to teach or suggest all of the limitations in claims 1, 4-6, 9-12 and 17 for at least the reasons presented below.

It is well-established law that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). Applicants assert that the rejection based on Schmidt does not meet this basic legal requirement, as will be explained below.

Amended independent claim 1 recites a method of checking the accuracy of a pseudorandom bit sequence (PRBS) received by a device, the method comprising the steps of: delaying the PRBS

received by the device to generate a delayed PRBS; detecting the presence of an error bit in the PRBS received by the device by comparing at least a portion of the delayed PRBS with at least a portion of the PRBS received by the device; and prohibiting propagation of the detected error bit in the delayed PRBS; wherein the detected error bit represents a mismatch between the delayed PRBS and the PRBS received by the device. Independent claims 6 and 11 recite similar limitations.

Further, original independent claim 12 recites apparatus for checking the accuracy of an output pseudorandom bit sequence (PRBS) generated by a device in response to an input PRBS received by the device, the apparatus comprising: a shift register chain; a logic gate coupled to the shift register chain and the device for detecting, for a given clock cycle, the presence of an error bit in the output PRBS, the error bit representing a mismatch between the input PRBS and the output PRBS; and at least one logic detector coupled to the logic gate for generating, in response to detection of the presence of the error bit, a logic value that causes the inversion of the error bit after waiting for a clock cycle so as to prohibit further propagation of the error bit through the shift register chain.

As illustratively explained in the present specification at page 4, line 14, through page 6, line 9, there are two major types of PRBS checkers. The first type uses a very simple technique as shown in FIG. 2 of the present application. PRBS checker 230 includes a synchronization detector (synchronizing circuit) 232, a local PRBS generator 234 and a comparator circuit 236. Synchronization detector 232 looks for a known pattern in the incoming stream. Once detector 232 detects the known pattern, detector 232 turns on local PRBS generator 234. Local generator 234 and the generator (e.g., 110 in FIG. 1, but not expressly shown in FIG. 2) at the input of DUT 220 are designed to be identical. After synchronization is achieved, the two generators are expected to produce identical bit streams. The comparator circuit 236 detects any mismatches caused due to DUT 220. A major drawback of this technique is the penalty caused due to the synchronizing circuit. These circuits are difficult to build, consume a lot of power as they run at the full rate of incoming data, and their size grows with the length of the generation polynomial.

Applicants respectfully point out that this first approach is the approach taken by Schmidt. The locally generated signal is the "test signal" described in Schmidt at column 4, lines 29-48.

A second approach uses a self-synchronizing technique as shown in FIG. 3 of the present application. This approach eliminates the need for a synchronizing circuit and local PRBS generation. As explained, PRBS generator 310 includes shift registers T0, T1 and T2, which form a shift register chain. The output of T2 and T1 is fed to an XOR (exclusive OR) gate TX0. The output of TX0 is fed to the input of register T0. Thus, a PRBS of length seven is formed. At any given time, there are three bits in the generator registers (T0 through T2). These three bits identify a single state out of seven states that the generator cycles through. Any new state can be derived from a previous state by the XOR and shift operation. This fundamental principle of generation is used in the self-synchronizing checker. PRBS checker 330 includes a shift register chain including R0, R1 and R2. Checker 330 also includes XOR gate RX0, XOR gate RX1 and error counter 332. The incoming bits from DUT 320 are shifted directly into the shift register chain which is of the same length as the generator shift register. The outputs of registers R2 and R1 in the receive side are then fed to XOR gate RX0. The output of RX0 is compared with the incoming bit. The comparison is done using XOR gate RX1. Under ideal circumstances, the incoming bit is the same as the RX0 output. Any errors introduced by DUT 320 are then counted by error counter 332.

As further explained in the present application, this second technique has three major drawbacks. First, multiple errors are flagged for a single occurrence. For example, if the DUT sends a bit stream with a single error bit, an error will be flagged at the output of XOR gate RX1 for the first time. This error bit will then propagate from the input of register R0 to the output of R1 after two clock events. When the erroneous bit arrives at the output of Rthe erroneous bit will flag an error for the second time. An error flag will be raised for the third time when this bit reaches the output of R2. Thus, a single error will be flagged three times. A second drawback is that the technique of FIG. 3 masks errors. For example, if in any given incoming stream there are two error bits separated by one, two or three bit positions, these will cancel each other, thus showing no error at all. This is referred to as masking.A third drawback of the technique of FIG. 3 is that if thDUT sends out only zero bits, no error is flagged.

A fundamental reason for flagging of multiple errors and masking is the propagation of an erroneous bit through the shift registers. The present invention realizes that to prevent such an occurrence, the error bit propagation has to be stopped. For example, in a binary system, this error bit can be inverted to its correct value.

The inventions recited in amended independent claims 1, 6 and 11, and original claim 12 address the stated problems with the existing self-synchronizing approach (FIG. 3) by "prohibiting propagation of the detected error bit in the delayed PRBS" (claims 1, 6 and 11), and by "at least one logic detector coupled to the logic gate for generating, in response to detection of the presence of the error bit, a logic value that causes the inversion of the error bit after waiting for a clock cycle so as to prohibit further propagation of the error bit through the shift register chain" (claim 12).

Schmidt clearly fails to disclose such a feature.

For at least the above reasons, Applicants assert that claims 1, 4-6, 9-12 and 17 are patentable over Schmidt.

Since Gilley, Manlick and Jungerman also fail to disclose such a feature, Applicants assert that dependent claims 2, 3, 7, 8 and 13-16 are patentable over any combinations including such references.

It is also asserted that one or more of the dependent claims of the present application recite separately patentable subject matter in their own right.

In view of the above, Applicants believe that claims 1-17 are in condition for allowance, and respectfully request withdrawal of the §102(b) and §103(a) rejections.

Respectfully submitted,

Date: March 31, 2006

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